

The diagram shows a 1T1R1C1M1S1 memory cell. It consists of a memory cell (MC) connected to word lines WWL and RWL, and bit lines LE and RWL. The memory cell is also connected to a sense amplifier (SA) via a voltage divider (VR) and a sense amplifier (SA). The output is connected to DIN and DOUT.

Timing diagram for a 1T1R1C1B1A1 memory array during a read operation. The diagram shows the signals RWL, WWL, RDL, LE, SO, and WDL over time. RWL is high during the first access. WWL is high during the first access and high again during the second access. RDL is high during the first access and high again during the second access. LE is high during the first access and high again during the second access. SO is high during the first access and high again during the second access. WDL is high during the first access and high again during the second access. The signals are labeled with 0, VDD, and VR.

FIG. 2A

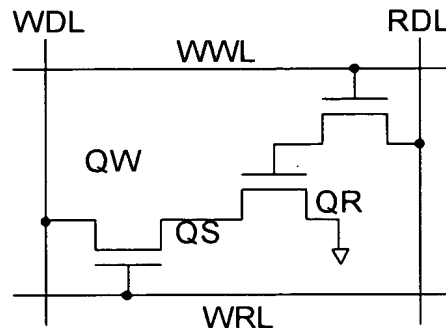


FIG. 2B

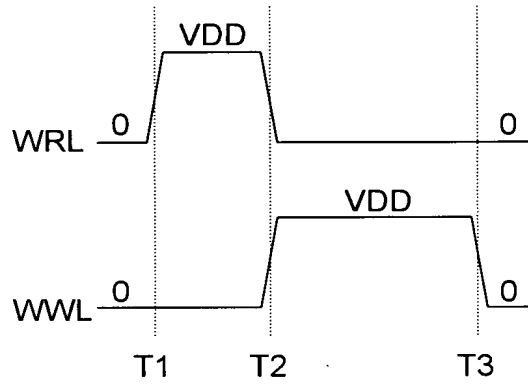


FIG. 2C

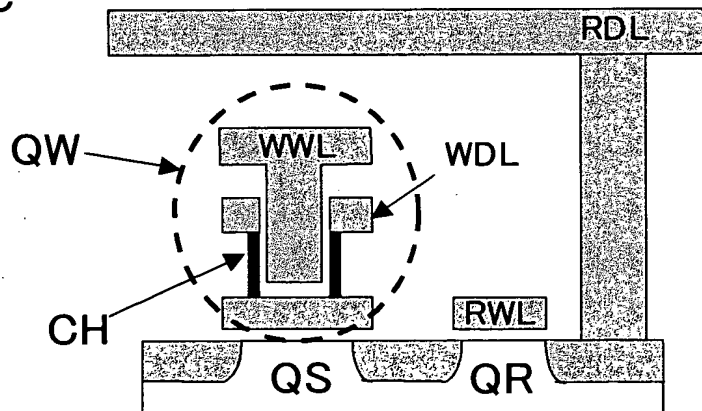


FIG. 3

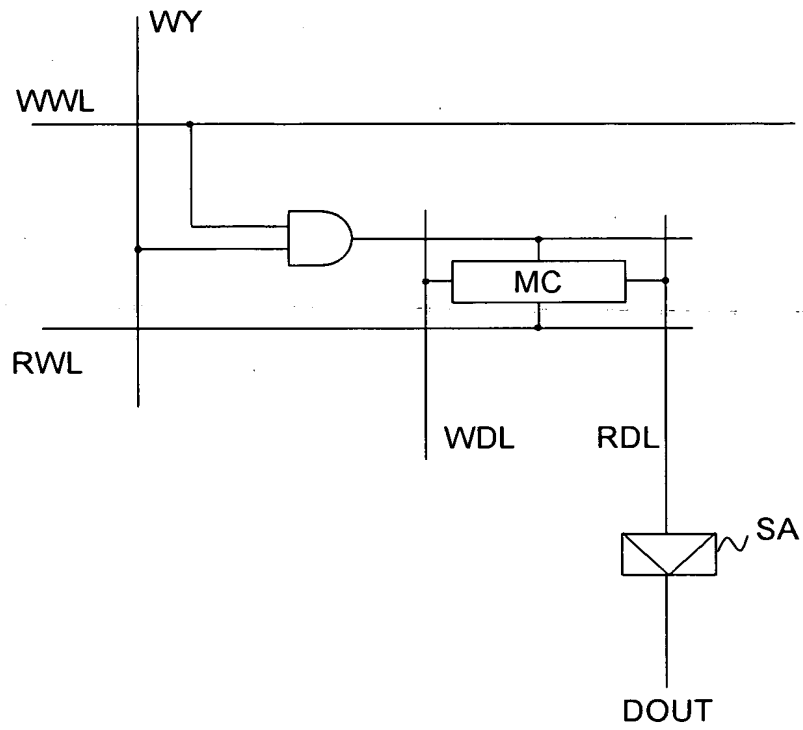


FIG. 4

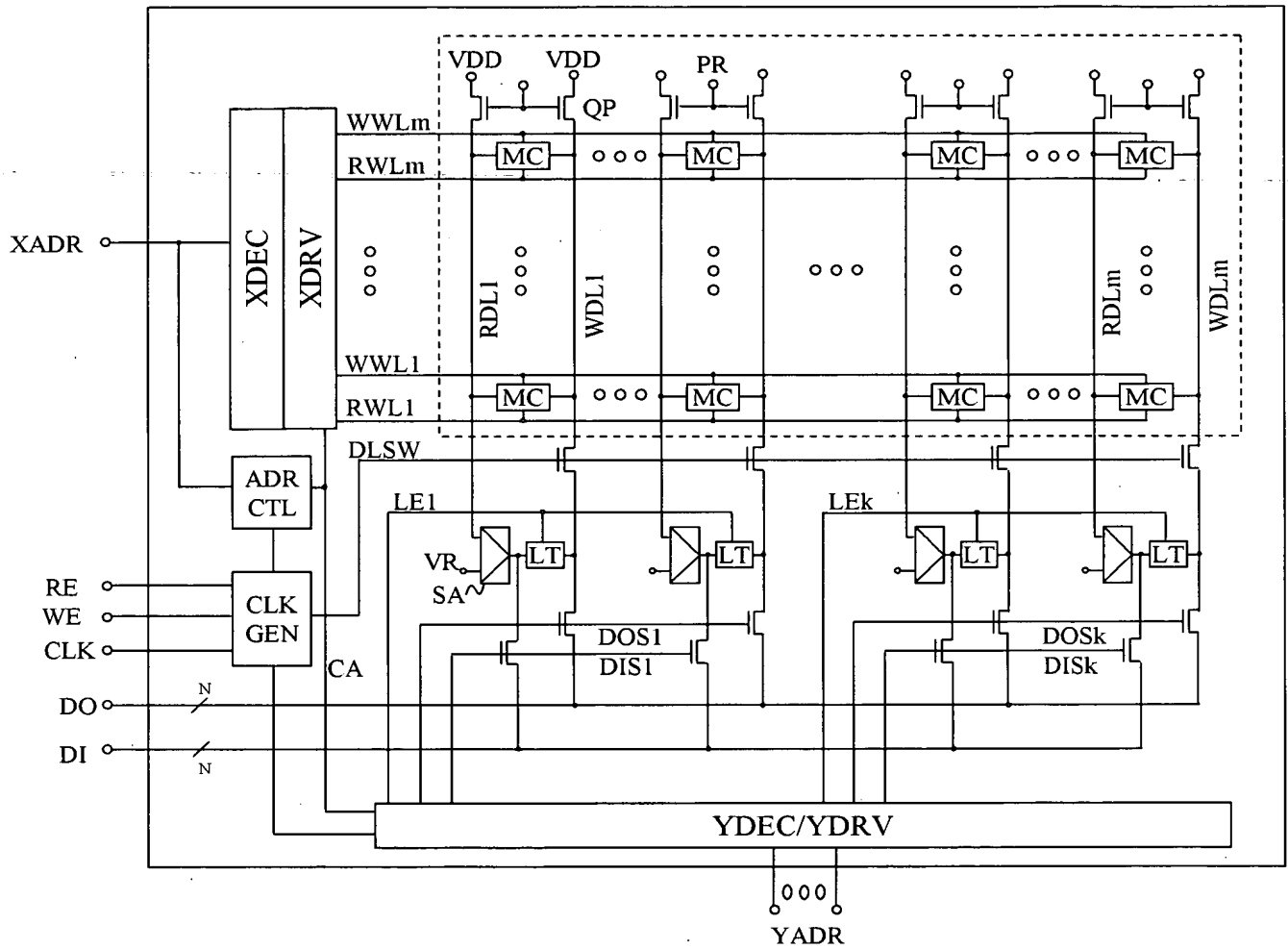


FIG. 5

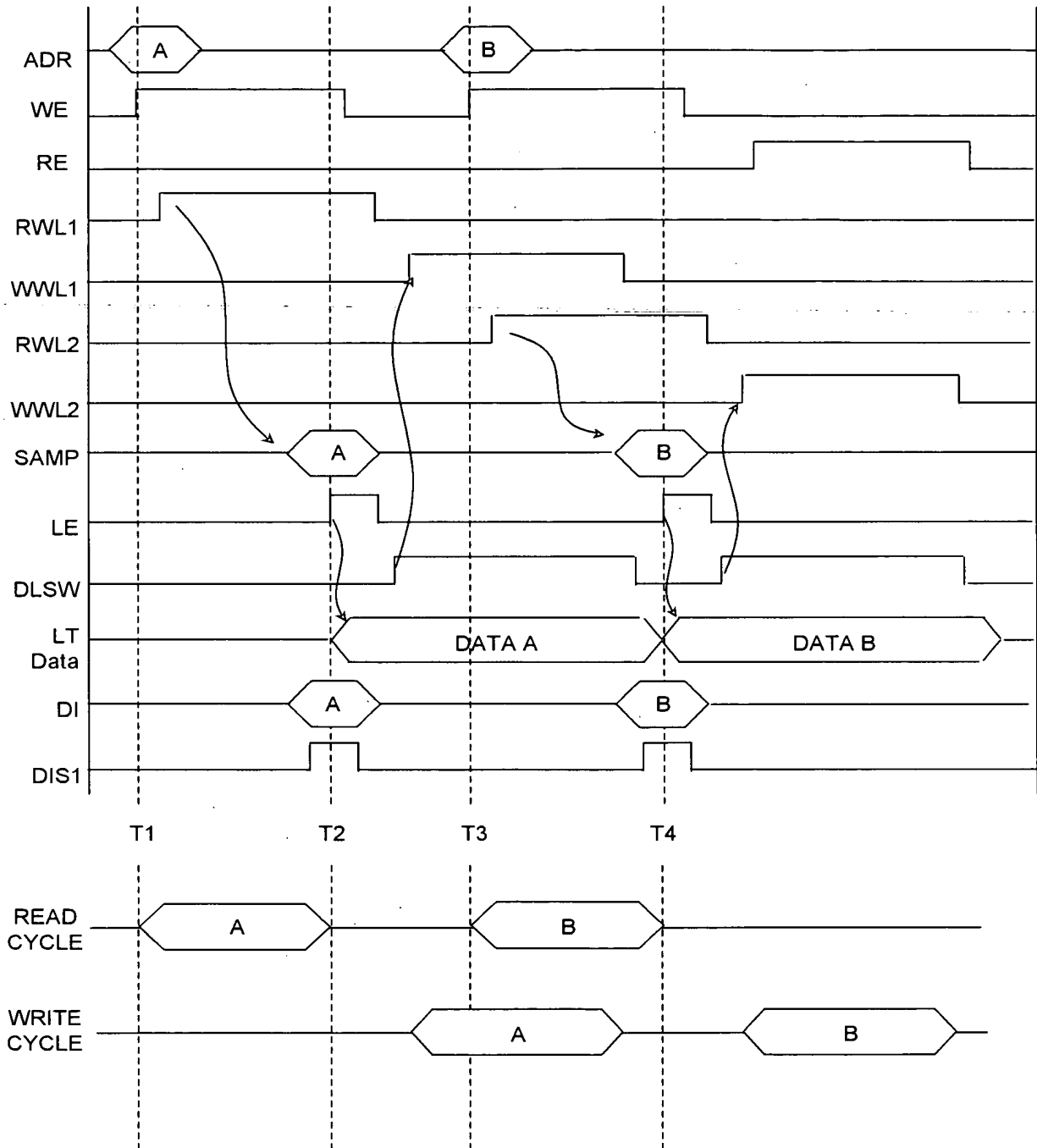


FIG. 6A

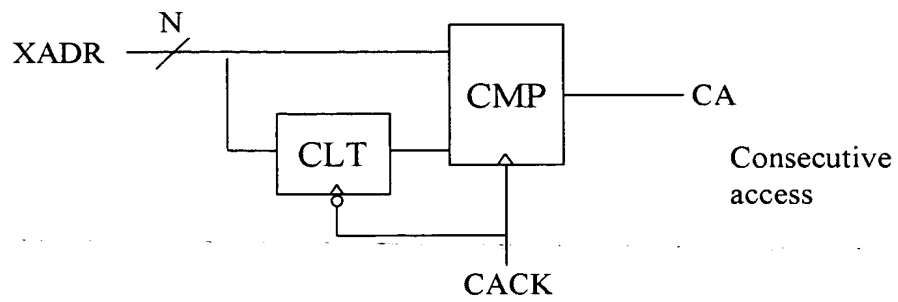


FIG. 6B

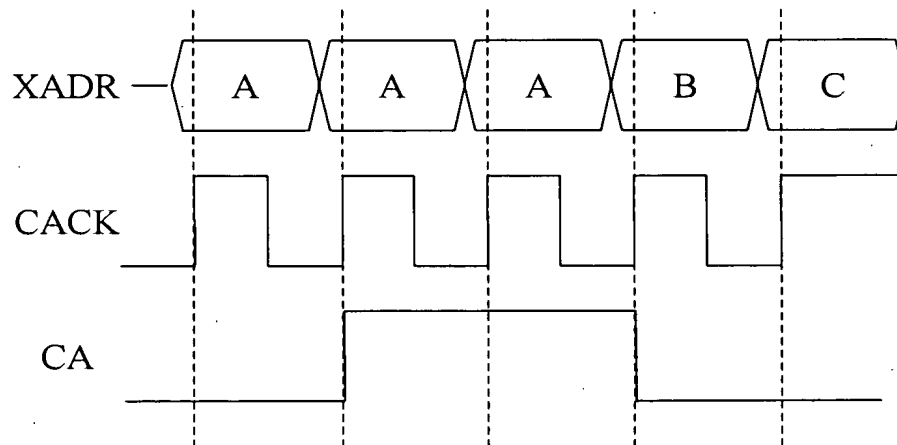


FIG. 7 (USE VISIO VERSION INSTEAD)

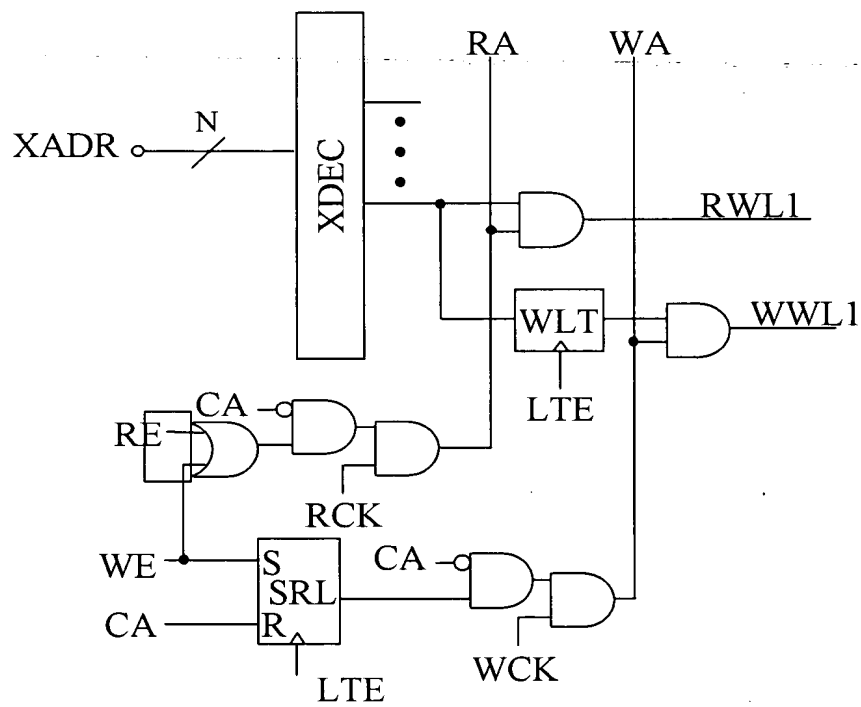


FIG. 8

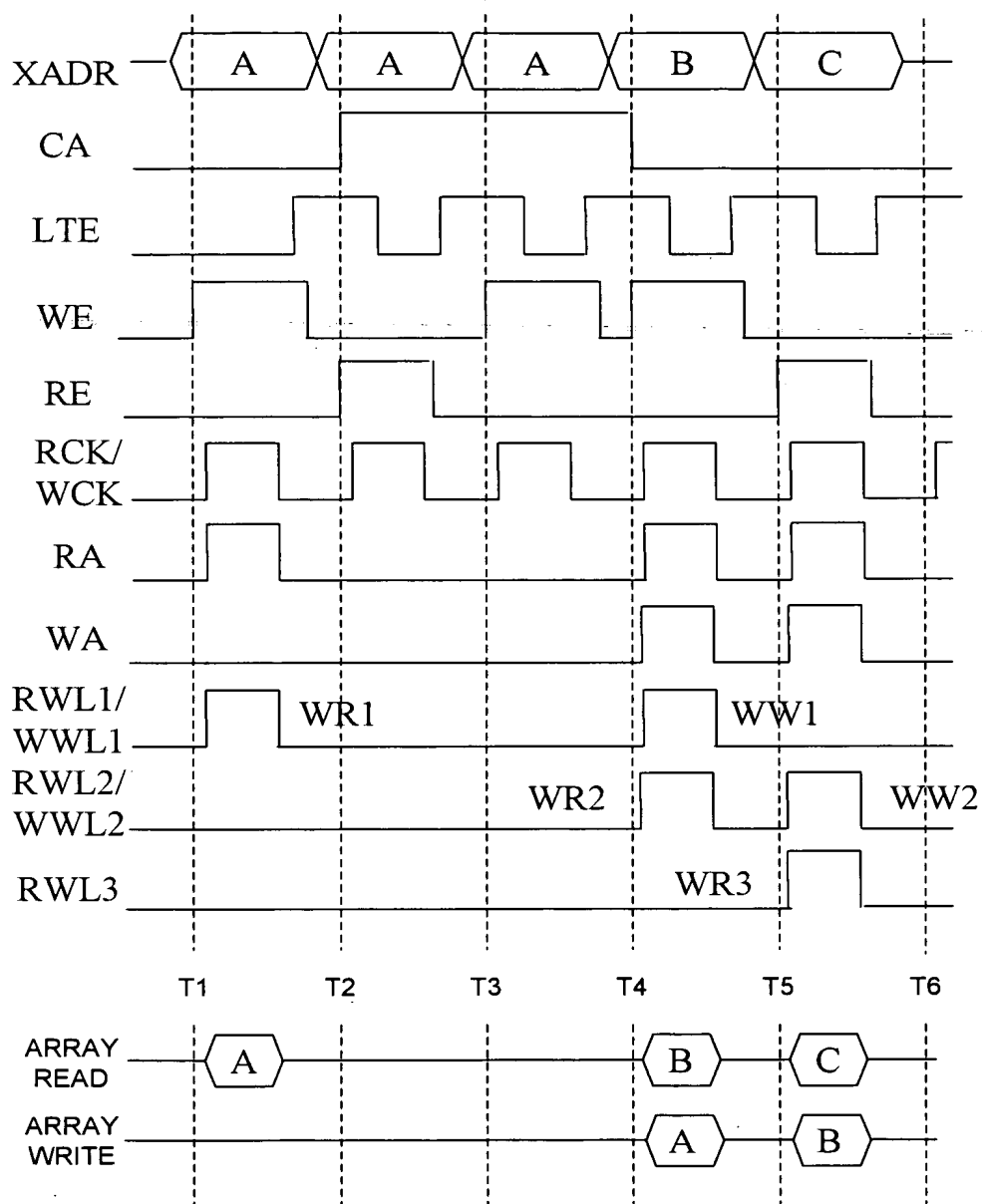


FIG. 9A (USE VISIO VERSION INSTEAD)

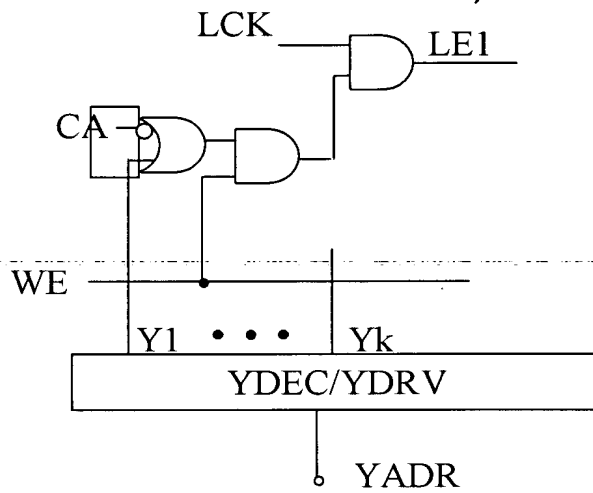


FIG. 9B

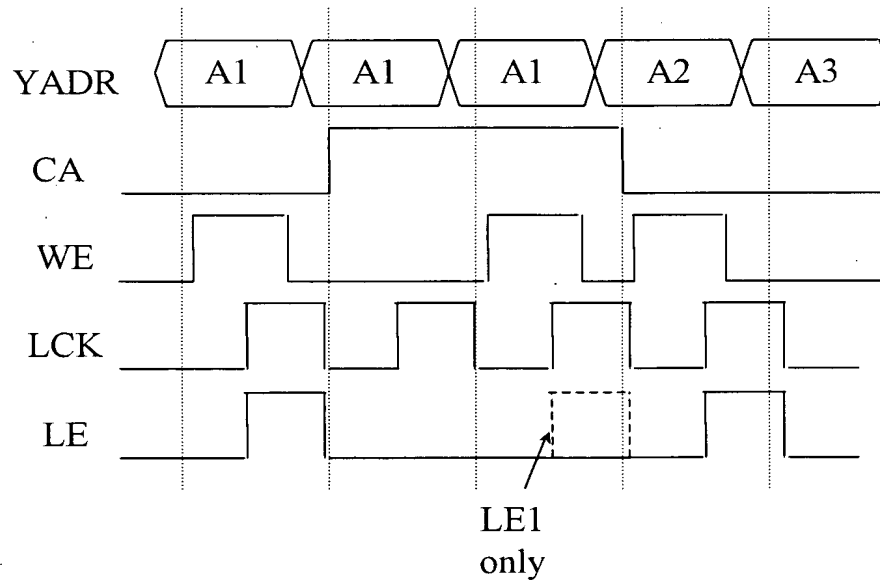


FIG. 10A

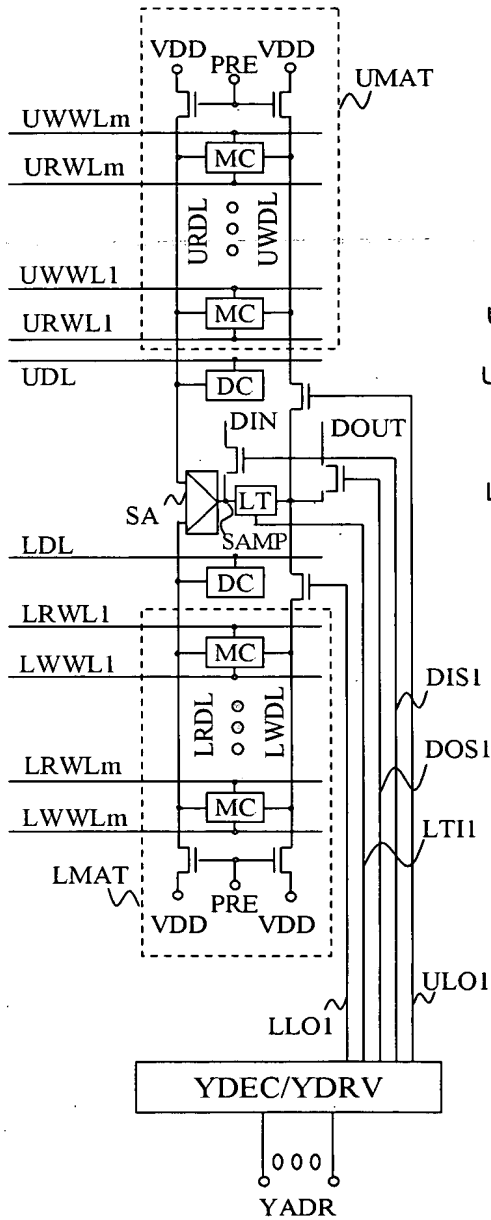


FIG. 10B

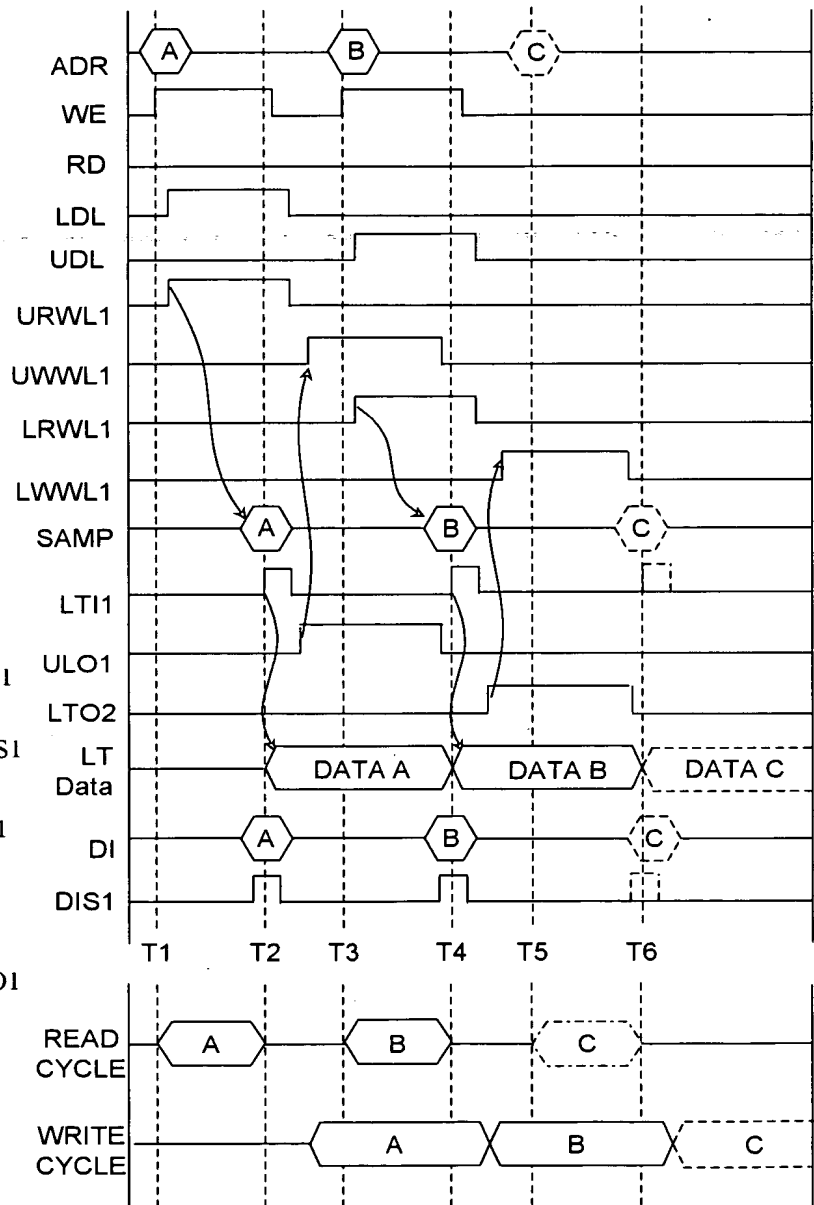


FIG. 11B

